EXPRESS MAIL NO.: EL872099148US

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Sion C. Quinlan et al.

Attorney Docket No.: 30022/US/2

Filed : concurrently herewith

Title : SEMICONDUCTOR PACKAGE ASSEMBLY AND METHOD FOR ELECTRICALLY ISOLATING MODULES

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

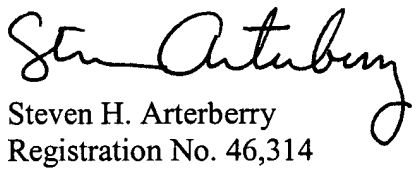
Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97 through 1.98, applicant wishes to make known to the Patent and Trademark Office the references set forth on the attached form PTO-1449. This application relies, under 35 U.S.C. § 120, on the earlier filing date of prior Application No. 10/057,205, filed January 25, 2002. The references listed on the attached Form PTO-1449 are enclosed as required under 37 C.F.R. § 1.98. Although the aforesaid references are made known to the Patent and Trademark Office in compliance with applicants' duty to disclose all information they are aware of which is believed relevant to the examination of the above-identified application, applicants believe that their invention is patentable.

Please acknowledge receipt of this Information Disclosure Statement and kindly make the cited references of record in the above-identified application.

Respectfully submitted,

DORSEY & WHITNEY LLP



Steven H. Arterberry
Registration No. 46,314

SHA:tlm

Enclosures:
Postcard
Form PTO-1449
Cited References (31)

1420 Fifth Avenue, Suite 3400
Seattle, WA 98101
Telephone (206) 903-8800
Facsimile (206) 903-8820

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 30022/US/2	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Sion C. Quinlan and Tim J. Bales	
		FILING DATE Concurrently Herewith	GROUP ART UNIT Not Yet Assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	AA	5,975,958	11-02-99	Weidler	439	620	
	AB	6,021,499	02/01/00	Aleshi	713	300	
	AC	6,023,202	02-08-00	Hill	333	24	
	AD	6,109,971	08-29-00	Vadlakonda	439	620	
	AE	6,124,756	09-26-00	Yaklin et al.	327	564	
	AF	6,147,542	11-14-00	Yaklin	327	344	
	AG	6,249,171 B1	06-19-01	Yaklin et al.	327	382	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	AH	00/45420	08/03/00	WO				
	AI	0 801 468 A2	10/15/97	EP				

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	AJ	Al-sarawi, Said F., "Wire Bonded Stacked Chips," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node35," January 25, 2002, pp. 1-2
	AK	Al-sarawi, Said F., "Blind Castellation Interconnection," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node44," January 25, 2002, p. 1
	AL	Al-sarawi, Said F., "Silicon Efficiency," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node20," January 25, 2002, pp. 1-2
	AM	Al-sarawi, Said F., "Delay," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node22," January 25, 2002, p. 1

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 30022/US/2	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Sion C. Quinlan and Tim J. Bales	
		FILING DATE Concurrently Herewith	GROUP ART UNIT Not Yet Assigned

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*		
	AN	Al-sarawi, Said F., "Noise," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node23," January 25, 2002, p. 1
	AO	Al-sarawi, Said F., "Power Consumption," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node24," January 25, 2002, p. 1
	AP	Al-sarawi, Said F., "Speed," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node25," January 25, 2002, p. 1
	AQ	Al-sarawi, Said F., "Interconnect Capacity," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node26," January 25, 2002, pp. 1-2
	AR	Al-sarawi, Said F., "Interconnection Capacity Between Packaging Levels," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node27," January 25, 2002, p. 1
	AS	Al-sarawi, Said F., "Stacked Tape Carrier," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node30," January 25, 2002, p. 1
	AT	Al-sarawi, Said F., "Solder Edge Conductors," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node31," January 25, 2002, pp. 1-2
	AU	Al-sarawi, Said F., "Thin Film Conductors on Face-of-a-Cube," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node32," January 25, 2002, pp. 1-2
	AV	Al-sarawi, Said F., "An Interconnection Substrate Soldered to the Cube Face," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node33," January 25, 2002, pp. 1-2

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 30022/US/2	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Sion C. Quinlan and Tim J. Bales	
		FILING DATE Concurrently Herewith	GROUP ART UNIT Not Yet Assigned

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*		
	AW	Al-sarawi, Said F., "Folded Flex Circuits," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node34," January 25, 2002, p. 1
	AX	Al-sarawi, Said F., "Area Interconnection Between Stacked ICs," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node36," January 25, 2002, p. 1
	AY	Al-sarawi, Said F., "Flip-chip Bonded Stacked Chips Without Spacers," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node37," January 25, 2002, p. 1
	AZ	Al-sarawi, Said F., "Flip-chip Bonded Stacked Chips With Spacers," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node38," January 25, 2002, p. 1
	BA	Al-sarawi, Said F., "Microbridge Springs and Thermomigration Vias," Centre for High Performance Integrated Technologies and Systems (CHIPTEC), March, 1997, obtained from website "http://www.eleceng.adelaide.edu.au/Personal/alsarawi/Packaging/node39," January 25, 2002, p. 1
	BB	Agere Systems – About 1394, "1394 – The High-Speed Serial Interface for All the Right Reasons/1394 Driver Support," obtained from website http://www.agree.com/1394/about.html," January 25, 2002, p. 1
	BC	Press Release Tuesday October 17, 2000, "Lucent Technologies introduces low-power IEEE-1394A chip for high-speed connection between PCs and consumer electronic devices," obtained from website http://www.lucent.com/press/1000/001017.mea.html," January 25, 2002, pp. 1-3
	BD	1394 Trade Association: Technology, "1394 Technology," obtained from website http://www.1394ta.org/Technology/," January 25, 2002, p. 1
	BE	1394 Trade Association: Technology, "An Introduction to the Instrument and Industrial Control Protocol," obtained at website http://www.1394ta.org/Download/Technology/iicpPaper2.pdf," January 25, 2002, 6 pages
	BF	Apple Computer, Inc., "Firewire Technology Fact Sheet," obtained at website "http://a772.g.akamai.net/7/772/51/f7f756ae8e5bf0/www.apple.com/firewire/pdf/FireWireFS-b.pdf", March 13, 2002, pp. 1-4
	BG	McMunn, Lee James, "The Physical Layer," obtained at website "http://www.awstevenson.demon.co.uk/SYSNOTES/physic.htm," March 12, 2002, pp. 1-2
	BH	Willis, P. J., "Communication Protocols," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/chapter2_6.html," August 17, 2001, p. 1

FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 30022/US/2	APPLICATION NO. Not Yet Assigned
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		APPLICANT(S) Sion C. Quinlan and Tim J. Bales	
		FILING DATE Concurrently Herewith	GROUP ART UNIT Not Yet Assigned

	BI	Willis, P. J., "The OSI Model," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/sections2_6_1.html," August 17, 2001, p.1
	BJ	Willis, P. J., "Physical Layer," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/subsection2_6_1_1.html," August 17, 2001, p. 1
	BK	Willis, P. J., "Data Link Layer," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/subsection2_6_1_2.html," August 17, 2001, p.1
	BL	Willis, P. J., "Network Layer," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/subsection2_6_1_3.html," August 17, 2001, p.1
	BM	Willis, P. J., "The Physical Layer," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/section2_7_1.html," August 17, 2001, pp. 1-2
	BN	Willis, P. J., "The Datalink Layer," obtained at website "http://www.maths.bath.ac.uk/~pjw/NOTES/networks/section2_7_2.html," August 17, 2001, pp. 1-2
	BO	Embedded Systems Programming, "Fundamentals of Firewire," obtained at website "http://www.embedded.com/1999/9906/9906feat2.htm," August 28, 2001, pp. 1-14
	BP	Microprocessor and Microcomputer Standards Committee of the IEEE Computer Society, "P1394a Draft Standard for a High Performance Serial Bus (Supplement)," The Institute of Electrical and Electronics Engineers, Inc., June 30, 1999, pp.1-27
	BQ	Lucent Technologies, Inc., "IEEE 1394 Isolation," Application Note, November 1998, obtained at website "http://www.agere.com/1394/docs/AP98074-01.pdf," pp. 1-16

EXAMINER	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).